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Innovative Architecture for FPGA based Multicore Hybrid Processor

Harisha M. S, D.Jayadevappa,

Abstract-- As we all know the Processor is heart and brain of today's computers, tab PC, mobile communications, medical electronics equipments etc., we undertook exhaustive data collections as a part of our literature survey and based on that we are proposing innovative architecture leading to multicore hybrid SOC. And we will model this Processor using Verilog and Xilinx ISE simulator. Also we intend to develop a rapid prototype using Xilinx FPGA as a part of research work.

Index Terms--Hybrid Processor, RISC, CISC, Processor Design, architectures, VLSI.

1. INTRODUCTION

We all are aware that Processor/CPU in a computer is equivalent to brain in human body. The Processor will direct the computer to perform basic operations like arithmetic, logic, input/output and also support for multitasking, parallelism, interrupts, interfacing, pipelining, software program support, plug and play drivers for new hardware, operating system interfacing etc., The term Processor has been in use in the computer industry at least since the early 1960s. The form design, and implementation of CPUs have changed over the course of their history, but their fundamental operation remains much the same. In older computers, CPUs require one or more printed circuit boards. With the invention of the Microprocessor, a CPU could be contained within a single silicon chip. The first computers to use Microprocessors were personal computers and small workstations. Since the 1970s the Microprocessor class of CPUs has almost completely overtaken all other CPU implementations, to the extent that even mainframe computers use one or more Microprocessors. Modern Microprocessors are large scale integrated circuits in packages typically less than four centimeters square, with hundreds of connecting pins.

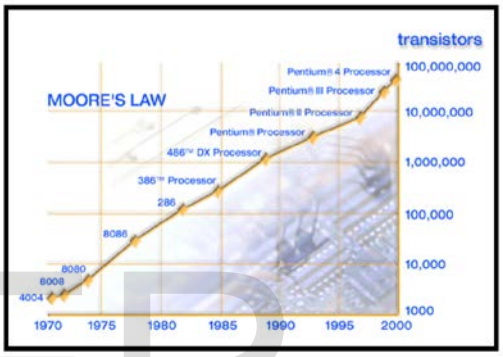

Fig 1 Moore's Law: 2x transistors every 18 months

The evolution of Processor is under rapid and vast innovations and implementations due to the requirement by end user.

From the above figure it can be observed that the as the Processor advancement increases from intel 4004 to pentium 4 the number of transistors also increased which leads to design complexity.

Processor

- logic capacity: about 30% increase per year
- clock rate: about 20% increase per year
- Higher logic density gave room for instruction pipeline & cache.

Memory

- DRAM capacity: about 60% increase per year (4x every 3 years).
- Memory speed: about 10%
- Cost per bit: about 25% improvement per year.

- *Harisha M. S, Research scholar in Electronics Engineering, Jain University, Bangalore, Karnataka, India.*
- *D.Jayadevappa, Professor, Dept. of Electronics & Inst. Engg, JSSATE, Bangalore, Karnataka, India.*

Performance optimization no longer implies smaller programs.

Disk

- Capacity: about 60% increase per year

Computers became lighter and more power efficient.

A computer can have more than one CPU; this is called multiprocessing. Some Microprocessors can contain multiple CPUs on a single chip; those Microprocessors are called Processors. Two typical components of a CPU are the arithmetic logic unit (ALU), which performs arithmetic and logical operations, and the control unit (CU), which extracts instructions from memory and decodes and executes them, calling on the ALU when necessary.

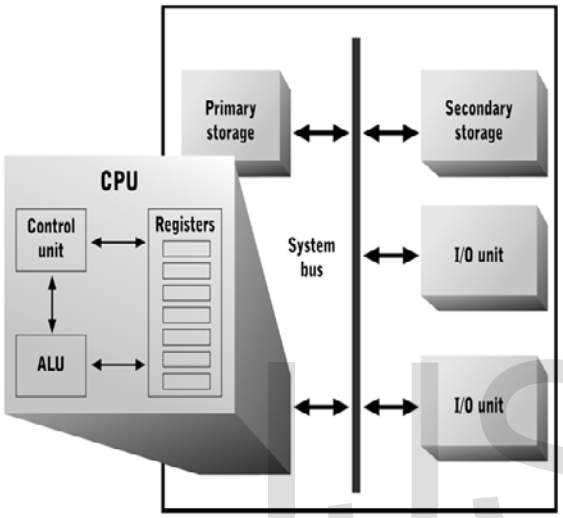

Fig 2: Components of central processing unit.

There are many applications of these Processor in many fields .They are:

- Microprocessor, a CPU on one silicon chip as part of a microcomputer.
- Application-specific instruction-set Processor, a component used in system-on-a-chip design.
- Graphics processing unit (GPU / VPU), a dedicated graphics rendering device for a personal computer or game console.
- Physics processing unit (PPU), a dedicated microprocessor designed to handle the calculations of physics.
- Digital signal Processor, a specialized Microprocessor designed specifically for digital signal processing.
- Network Processor, a Microprocessor specifically targeted at the networking application domain.
- Front end Processor, a helper Processor for communication between a host computer and other devices.
- Coprocessor.
    - Floating-point unit.
- Data processing system, a system that translates or converts between different data formats.
- Word Processor, a computer application used for the production of printable material.
- Audio Processor, used in studios and radio stations.
- Food Processor, an appliance used to facilitate repetitive tasks in the preparation of food.
- Numeric data Processor, for mobile communications.
- Fuzzy logic Processor, for washing machines, automatic vehicle movement, automatic aero plane movement

All these applications of Processor in different fields confirms us there is a need of Processor in every fields where the computational aspects to be done with required advancement of existing one.

Fig 3: Applications of Processor.

2. RISC AND CISC

From the architecture point of view, the Microprocessor can be classified into two categories: Complex Instruction Set Computers (CISC) and Reduce Instruction Set Computers (RISC).

1.1 HISTORY OF RISC and CISC

RISC methodology was developed at IBM in the late 1960s before Microprocessors were even invented. Yet despite that, until recent times, all of the major manufacturers of Microprocessors used CISC based designs.

The reason for this is that Microprocessors were introduced in the early 1970s to be used in simple electronic products such as calculators, stereos and video games, not personal computers. CISC technology was more suitable for this application.

Eventually these CISC based Microprocessors found their way into personal computers. The PCs evolved with generation after generation of CISC based

Microprocessors being introduced to meet the ever increasing demands of PC users. The Microprocessor manufacturers began to refocus their CISC Microprocessor design efforts away from general purpose designs to a high-performance computing orientation.

From the study history of Processor till today's recent Processor there is an argument that the we are in "Post RISC" era, where the CISC Processor are designed by keeping RISC features as foundation a very good example is Intel core 2 Duo.

1.2 RISC Architecture

The popular RISC Architecture of PIC is shown in Fig 4 which has the following features:

- I/O Interfacing.
- Register to Register transfer.
- Harvard Architecture.
- Different bus widths of data and program memory.
- Machine cycle consist of 4 clock pulses.
- Instruction set is highly orthogonal.
- Watch Dog timer (WDT)
- Power on Reset. (POR)
- Brown out Reset (BOR).
- Capture/Compare/ PWM modules.
- USART
- Synchronous serial port (SSP) with SPI and I2C.
- Power saving SLEEP mode.

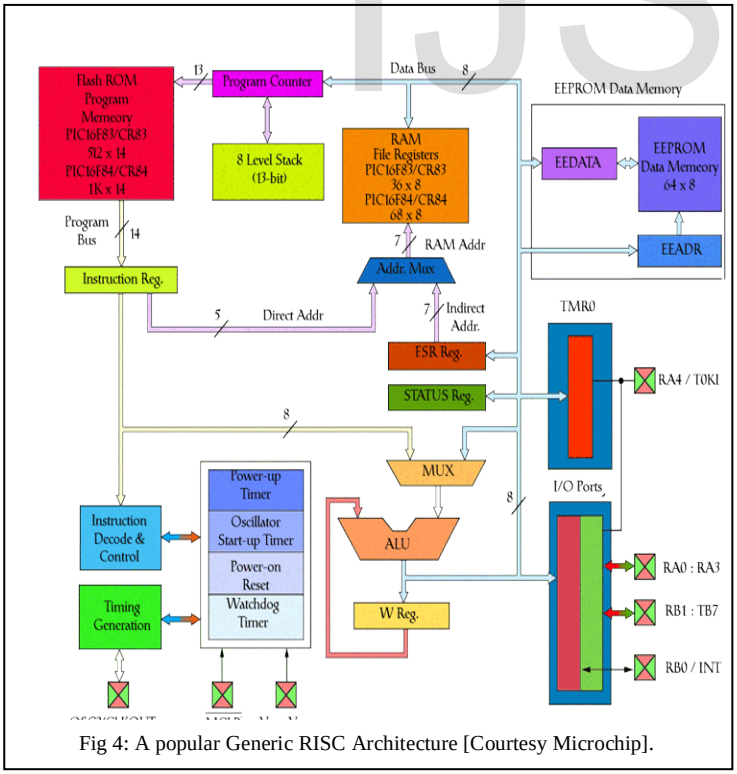

Fig 4: A popular Generic RISC Architecture [Courtesy Microchip].

1.2 CISC Architecture

The generic CISC Architecture is shown in Fig 5 have following features:

- Interrupts.
- Memory to Memory transfer.
- General purpose Registers.
- External Interfacing.
- Pipelining.
- Higher Throughput.
- It has multiplexed address and data bus due to which the pin count is reduced considerably.
- 16-bit ALU.
- It can be used with math coprocessors.
- It has 16-bit data bus, so it can read data or write data to memory or I/O ports either 16 bits or 8 bits at a time.
- It has 20 address lines, so it can address up to 220 i.e. 1048576 = 1Mbytes of memory

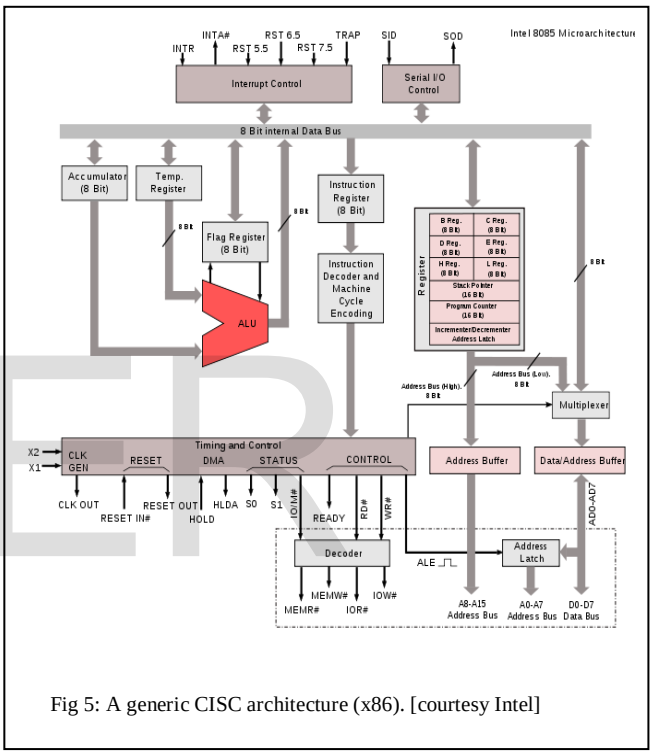

Fig 5: A generic CISC architecture (x86). [courtesy Intel]

RISC V/s CISC

TABLE 1
RISC AND CISC

CISC	RISC
Price/Performance Strategies	

Price: move complexity from software to hardware. **Performance: make tradeoffs in favor of decreased code size, at the expense of a higher CPI (Cycles/instructions).**	Price: move complexity from hardware to software Performance: make tradeoffs in favor of a lower CPI, at the expense of increased code size.
Design decisions	
• **A large and varied instruction set that includes simple, fast instructions.** • **Support for HLLs is done in hardware.** • **Memory-to-memory addressing modes.** • **Spend fewer transistors on registers.** • **No pipelining** • **Use micro Encoding of the machine instructions.** **Eg: intel's Processors, AMD Processors.**	• Simple, single-cycle instructions that perform only basic functions. • All HLL support is done in software. • Simple addressing modes that allow only LOAD and STORE to access memory. All operations are register-to-register. • spend more transistors on multiple banks of registers. • use pipelined execution to lower CPI. • Use hardwired control unit of machine instructions. Eg: Apple's Processor, ARM Processors

2 PROCESSOR DESIGN

2.1 Key Issues

The Processor design has many issues to be considered. They are as follows:

- ✓ Best RISC features
- ✓ Best CISC features
- ✓ Instruction set Architectures
- ✓ Multitasking
- ✓ Multicore Processors
- ✓ Memory management
- ✓ addressing modes
- ✓ Timing
- ✓ Power
- ✓ Clock
- ✓ Ports
- ✓ I/O Interfacing
- ✓ Bus
- ✓ Interrupts
- ✓ Interfacings
- ✓ parallelism
- ✓ pipelining
- ✓ Benchmarks

Keeping the above issues as the base an efficient Hybrid Processor with the best features of RISC and CISC can be proposed.

3 NEED FOR HYBRID PROCESSOR

Recent advancement in Processor which performs fast execution can be of multicore type. Since as the level of computation increased the need for fast and cost effective Processor is must required, cost and performance are two Processor constraints. Later on the multi core with same type of cores will also fail to meet the constraints. So there is a need for even more, even more when it comes to Processor selection. An efficient utilization of two different architecture is come in it picture, which is called HYBRID Processor the mix and match of best features of RISC standalone core and CISC standalone core (dual core).

4 PROPOSED HYBRID PROCESSOR

The hybrid Processor which will be designed and proposed having,

- ✓ Number of bits -16 bit (scalable upto 256 bit).
- ✓ Speed 1MHz-100MHz.
- ✓ Instruction set-Subset of RISC & CISC (32-48).
- ✓ Relevant addressing modes.
- ✓ Interrupts best possible.
- ✓ Interfacing-LCD,LED,BUZZER,RF-smartcard, GSM, keyboard etc.,
- ✓ Built-in Memory interface.
- ✓ Ports-UART.
- ✓ I/O switches.

The proposed Hybrid architecture will be prototyped tested on FPGA first and later after intense optimization, field trails, testing and fabrication process will be leading to a SOC (ASIC).

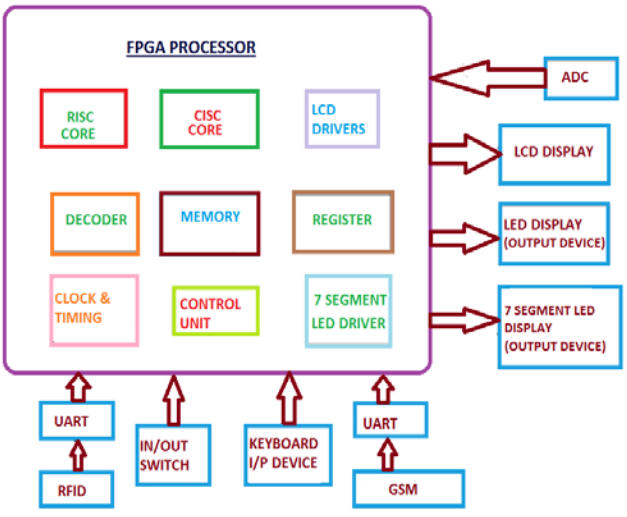

Fig 6 : Proposed Hybrid Processor Architecture

The small FPGA prototype hybrid Processor will have a subset of the total features of a full fledge Processor of high speed high performance (low power, low cost).

4.1 Methodology

Neither RISC nor CISC standalone Processor can produce a complete solution to the present day computational needs, hence there is a strong need of hybrid Processor. Our proposed architecture will utilize all the best features of both RISC and CISC.

4.2 Why FPGA?

- Low cost rapid prototype hardware platform.
- Complete support for hardware modeling (behavioral simulation and RTL synthesis).
- Shortened development time.
- Reprogrammablity and Low NRE cost.
- Programmability and scalability and flexibility.
- Field up gradation.
- High density, high speed, low power.
- Shortened time of design changes.

5 CONCLUSIONS

Keeping all above said technical issues in mind we aim to develop a multi core (dual) hybrid Processor which will take the advantage of the best features of both RISC and CISC. The biggest challenge in such a Processor design and implementation would be judicious allocation of resources like:

1. Memory
2. Bus
3. Instructions
4. Speed
5. Power
6. Overall Cost
7. Overall Resource Management
8. Interfaciability
9. Parallelism/Multitasking.

REFERENCES

[1] John L. Hennessy, and David A. Patterson, “Computer Architecture A Quantitative Approach”, 4th Edition; 2006.
[2] Radha Krishnan and rajaraman “Digital computer design” ,fifth edition,PHI,2009
[3] Niklaus Wirth, “The Design of a RISC Architecture and its Implementation with an FPGA”,2011.
[4] Imran Mohammad, Ramananjaneyulu K, Dr. K. Veeraswamy, “FPGA Implementation of a 64-Bit RISC Processor Using VHDL”, IJERA, Vol. 2, Issue 3, pp.2544-2549, May-Jun 2012.
[5] Masatoshi Shima “The 4004 CPU of my Youth”,IEEE solid state magazine,2009.
[6] V.N.Sireesha , D.Hari Hara Santosh, “FPGA Implementation of A MIPS RISC Processor”, Int.J.Computer Technology & Applications,Vol 3 (3), 1251-1253.
[7] Michael Freeman, “A Minimal CISC Processor Architecture for Field Programmable Gate Arrays”.
[8] Hasan Krad and Aws Yousif Al-TaieDepartment “A New Trend for CISC and RISC Architectures”
[9] Processor informations [Online]. Available: www.intel.com.
[10] Niklaus Wirth, “Experiments in Computer System Design”, Technical Report, august 2010.